IN THE CLAIMS:

Cancel claims 1-3 and add new claims 4-16 as shown in the following listing of claims, which replaces all previous listings and versions of claims.

4. (new) A flip-flop circuit comprising:

a data input terminal;

a first switching element having a first terminal connected to the data input terminal, a second terminal, and a first gate for receiving a first control signal;

a first inverter element having an input terminal connected to the second terminal of the first switching element and an output terminal;

a second switching element having a first terminal connected to the output terminal of the first inverter element, a second terminal, and a second gate for receiving a second control signal;

a second inverter element having an input terminal connected to the second terminal of the second switching element and a data output terminal; and

signal generating means for generating the first and second control signals and for inputting the first and second control signals to the first and second gates of the first and second switching elements, respectively, to simultaneously

activate the first and second switching elements for initializing the flip-flop circuit and to alternately activate the first and second switching elements for activating the flip-flop circuit.

5. (new) A flip-flop circuit according to claim 4; wherein each of the first and second switching elements comprises an NMOS transistor.

6. (new) A flip-flop circuit according to claim 4; further comprising a first MOS transistor having a gate terminal connected to the output terminal of the first inverter element and a drain connected to the input terminal of the first inverter element; and a second MOS transistor having a gate terminal connected to the output terminal of the second inverter element and a drain connected to the input terminal of the second inverter element.

7. (new) A flip-flop circuit according to claim 6; wherein each of the first and second switching elements comprises an NMOS transistor.

8. (new) A shift register comprising: a plurality of flip-flop circuits according to claim 4 connected in series.

9. (new) A method for operating a flip-flop circuit, comprising the steps of:

providing a flip-flop circuit comprising a data input terminal; a first switching element having a first terminal connected to the data input terminal, a second terminal, and a first gate for receiving a first control signal; a first inverter element having an input terminal connected to the second terminal of the first switching element and an output terminal; a second switching element having a first terminal connected to the output terminal of the first inverter element, a second terminal, and a second gate for receiving a second control signal; and a second inverter element having an input terminal connected to the second terminal of the second switching element and a data output terminal;

initializing the flip-flop circuit by inputting first and second control signals to the first and second gates of the first and second switching elements, respectively, to simultaneously activate the first and second switching elements; and

activating the flip-flop circuit by inputting the first and second control signals to the first and second gates of the first and second switching elements, respectively, to alternately activate the first and second switching elements.

10. (new) A method according to claim 9; wherein each of the first and second switching elements of the flip-flop circuit comprises an NMOS transistor.

11. (new) A method according to claim 9; wherein the flip-flop circuit further comprises a first MOS transistor having a gate terminal connected to the output terminal of the first inverter element, a drain connected to the input terminal of the first inverter element, and a source connected to a power supply; and a second MOS transistor having a gate terminal connected to the output terminal of the second inverter element, a drain connected to the input terminal of the second inverter element, and a source connected to a power supply.

12. (new) A method according to claim 11; wherein each of the first and second switching elements of the flip-flop circuit comprises an NMOS transistor.

13. (new) A method for operating a shift register, comprising the steps of:

providing a plurality of flip-flop circuits connected together, each of the flip-flop circuits comprising a data input terminal; a first switching element having a first terminal connected to the data input terminal, a second terminal, and a first gate for receiving a first control

signal; a first inverter element having an input terminal connected to the second terminal of the first switching element and an output terminal; a second switching element having a first terminal connected to the output terminal of the first inverter element, a second terminal, and a second gate for receiving a second control signal; and a second inverter element having an input terminal connected to the second terminal of the second switching element and a data output terminal;

initializing the shift register by inputting first and second control signals to the first and second gates of the first and second switching elements, respectively, of each of the flip-flop circuits to simultaneously activate the first and second switching elements; and

activating the shift register by inputting the first and second control signals to the first and second gates of the first and second switching elements, respectively, of each of the flip-flop circuits to alternately activate the first and second switching elements.

14. (new) A method according to claim 13; wherein each of the first and second switching elements of each of the flip-flop circuits comprises an NMOS transistor.

15. (new) A method according to claim 13; wherein each of the flip-flop circuits further comprises a first MOS transistor having a gate terminal connected to the output terminal of the first inverter element and a drain connected to the input terminal of the first inverter element; and a second MOS transistor having a gate terminal connected to the output terminal of the second inverter element and a drain connected to the input terminal of the second inverter element.

16. (new) A method according to claim 15; wherein each of the first and second switching elements of each of the flip-flop circuit comprises an NMOS transistor.